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Continuity Information for 10/033768

Parent Data10033768is a continuation in part of 09563784**Child Data**PCT/US02/39835 is a continuation of 10033768

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Application Number Information

Application Number: **09/563784**
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Filing Date: **04/29/2000**Effective Date: **04/29/2000**Application Received: **05/01/2000**Patent Number: **6508883**Issue Date: **01/21/2003**Date of Abandonment: **00/00/0000**Attorney Docket Number: **464**Status: **150 /PATENTED CASE**Confirmation Number: **7758**Title of Invention: **THROUGHPUT ENHANCEMENT FOR SINGLE WAFER REACTOR**Examiner Number: **72222 / LUND, JEFFRIE**Group Art Unit: **1763**Class/Subclass: **118/728.000**Lost Case: **NO**

Interference Number:

Unmatched Petition: **NO**L&R Code: Secrecy Code:**1**Third Level Review: **NO** Secrecy Order: **NO**Status Date: **01/02/2003**

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	4.Film thickness distribution control with off-axis circular		

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<input type="checkbox"/>	77%	<u>5.An indium-free substrate holder for radiative heating of quarter-wafer molecular-beam epitaxy samples</u> PDF (398 kB) GZipped PS Order	K. J. Kuhn	Rev. Sci. Instrum. 61 , 184 (1990)
<input type="checkbox"/>	77%	<u>6.Shape of a substrate holder for depositing coatings of uniform thickness</u> Order	A. V. Kondratov, A. I. Postnikov, and A. A. Potapenko	Sov. Phys. Tech. Phys. 26 , 515 (1981)
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<input type="checkbox"/>	77%	<u>8.Thickness Distribution and Step Coverage in a New Planetary Substrate Holder Geometry</u> PDF (1197 kB) GZipped PS Order	Klaus H. Behrndt	J. Vac. Sci. Technol. 9 , 995 (1972)

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Concomitant modifications were made in the tools and control logic in the existing rotation and wafer transfer sub-system.

Over 200 dual wafer transfers were performed with no operational problems. The ability to deposit thin films onto two substrates simultaneously in the single substrate reactor effectively doubled the throughput, over sequential processing of single wafers. This resulted in a dramatic reduction in manufacturing costs, while retaining the significant advantages of uniformity and reproducibility of the thin film deposition.

The present invention extends to and encompasses other features, modifications, and alternative embodiments, as will readily suggest themselves to those of ordinary skill in the art based on the disclosure and illustrative teachings herein. The claims that follow are therefore to be construed and interpreted as including all such features, modifications and alternative embodiments, within their spirit and scope.

What is claimed is:

1. A semiconductor substrate processing system, comprising:
 - a reactor comprising a single substrate deposition chamber;
 - a wafer holder positionable in said deposition chamber, said wafer holder being of plate-like form, and having a plurality of recesses formed therein, wherein n is the number of recesses, to coplanarly hold a corresponding number n of wafers, with a center-to-center distance between adjacent wafers determined by center-to-center spacing between recesses holding said adjacent wafers;
 - a substrate cassette coplanarly holding a corresponding number n of wafers therein, wherein wafers coplanarly adjacent to one another have a center-to-center spacing therebetween equal to said center-to-center distance between adjacent wafers in said wafer holder; and
 - an automated substrate transport assembly comprising a corresponding number n of coplanar wands, wherein wands coplanarly adjacent to one another have a center-to-center spacing therebetween equal to said center-to-center distance between adjacent wafers in said wafer holder,
2. The system of claim 1, wherein the automated substrate transport assembly are constructed and arranged for simultaneous coplanar loading of said n wafers from the substrate cassette into said n recesses in the wafer holder, simultaneous processing of said n wafers in the wafer holder in the single substrate deposition chamber, and simultaneous coplanar transport of said n wafers from the wafer holder.
3. The system of claim 1, wherein said coplanar wands in the automated substrate transport assembly comprise double-sided coplanar wands.
4. The system of claim 1, further comprising a loadlock chamber for containing the substrate cassette.
5. The system of claim 1, wherein n is 2.
6. The system of claim 1, wherein n is 4.
7. The system of claim 1, wherein the wafer holder has a diameter in the range of about 200 mm to about 350 mm.
8. The system of claim 1, wherein the wafer holder has a diameter in the range of from about 200 mm to about 300 mm.
9. The system of claim 1, wherein each of the wafer holder recesses has a diameter in the range of from about 100 mm to about 150 mm.
10. The system of claim 1, wherein each of the wafer holder recesses has a diameter in the range of from about 100 mm to about 125 mm.
11. The system of claim 1, wherein the single wafer deposition chamber is sized for processing single substrates having a 200 mm diameter.
12. The system of claim 1, wherein the wafer holder holds 100 mm diameter wafers.
13. The system of claim 1, wherein each of the recesses formed in the wafer holder is circular.
14. The system of claim 1, further comprising a processor for programmably operating the automated substrate transport assembly according to a cycle time program.
15. A method of increasing the throughput of a semiconductor processing system including a reactor comprising a single substrate deposition chamber, said method comprising:
 - positioning in said deposition chamber a wafer holder of plate-like form, having a plurality of recesses formed therein, wherein n is the number of recesses, to coplanarly hold a corresponding number n of wafers, with a center-to-center distance between adjacent wafers determined by center-to-center spacing between recesses holding said adjacent wafers;
 - providing a substrate cassette coplanarly holding a corresponding number n of wafers therein, wherein wafers coplanarly adjacent to one another have a center-to-center spacing therebetween equal to said center-to-center distance between adjacent wafers in said wafer holder;
 - providing an automated substrate transport assembly comprising a corresponding number n of coplanar wands, wherein wands coplanarly adjacent to one another have a center-to-center spacing therebetween equal to said center-to-center distance between adjacent wafers in said wafer holder,
 - operating the wafer holder, substrate cassette and automated substrate transport assembly for simultaneous coplanar loading of said n wafers from the substrate cassette into said n recesses in the wafer holder, simultaneous processing of said n wafers in the wafer holder in the single substrate deposition chamber, and simultaneous coplanar transport of said n wafers from the wafer holder.
16. The method of claim 15, further comprising positioning the substrate cassette in a substrate pickup and substrate delivery relationship to the automated substrate transport assembly.
17. The method of claim 16, further comprising translating the automated substrate transport assembly into a pickup position relative to the substrate cassette, so that the said corresponding number n of coplanar wands engage and extract said corresponding number n of wafers from the substrate cassette, with each wand engaging and extracting a respective wafer from the substrate cassette.
18. The method of claim 16, further comprising translating the automated substrate transport assembly into a pickup position relative to the substrate cassette, so that the said corresponding number n of coplanar wands engage and extract said corresponding number n of wafers from the substrate cassette, with each wand engaging and extracting a respective wafer from the substrate cassette;

translating the automated substrate transport assembly to a deposit position relative to the substrate cassette; releasing from the corresponding number n of coplanar wands the corresponding number n of wafers on the substrate cassette;

depositing thin film material on the corresponding number n of wafers in the deposition chamber, to yield the corresponding number n of coated wafers;

translating the automated substrate transport assembly into a pickup position after the depositing step is completed, and extracting the corresponding number n of coated wafers from the respective recesses in the wafer holder;

translating the automated substrate transport assembly carrying the corresponding number n of coated substrates into a deposit position relative to said substrate cassette or a second substrate cassette; and

releasing the corresponding number n of coated substrates to said substrate cassette or a second substrate cassette.

18. The method of claim 15, wherein said coplanar wands in the automated substrate transport mechanism comprise double-sided coplanar wands.

19. The method of claim 15, comprising sequentially using multiple wafer holders including positioning one of the multiple wafer holders in the deposition chamber for processing of wafers thereon, and concurrently regenerating another of said wafer holders after it has been in the deposition chamber.

20. The method of claim 19, wherein said regenerating comprises etch processing of said another of said wafer holders.
21. The method of claim 15, wherein n is 2.
22. The method of claim 15, wherein n is 4.
23. The method of claim 15, wherein the wafer holder has a diameter in the range of from about 200mm to about 350mm.
24. The method of claim 15, wherein the wafer holder has a diameter in the range of from about 200 mm to about 300 mm.
25. The method of claim 15, wherein each of the wafer holder recesses has a diameter in the range of from about 100 mm to about 150 mm.
26. The method of claim 15, wherein each of the wafer holder recesses has a diameter in the range of from about 100 mm to about 125 mm.
27. The method of claim 15, wherein the single wafer deposition chamber is sized for processing single substrates having a 200 mm diameter.
28. The method of claim 15, wherein the wafer holder holds 100 mm diameter wafers.
29. The method of claim 15, wherein each of the recesses formed in the wafer holder is circular.
30. The method of claim 15, further comprising providing a processor for programmably operating the automated substrate transport assembly according to a cycle time program.

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1	1	us-20020170673-\$.did.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 10:45
8	8928	(wafer or substrate or article) with shelves	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 10:47
15	8928	(wafers or substrates or articles) with shelves	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 10:47
22	1088	(wafer or substrate or article) with (shelves and (holder or rack or susceptor)) <i>↳ or bent see below --</i>	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 12:24
29	153	((wafer or substrate or article) with (shelves and (holder or rack or susceptor))) and robot	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 11:23
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50	18	(semiconductor with (shelves and (holder or rack or susceptor))) and (wafer or substrate or article) not (((wafer or substrate or article) with (shelves and (holder or rack or susceptor))) and robot)	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 11:33
57	6538	((glass or 'sio.sub.2' or "silicon dioxide" or silica or quartz) with ((holder or rack or susceptor))) and (wafer or substrate or article) not (((wafer or substrate or article) with (shelves and (holder or rack or susceptor))) and robot) <i>↳ or bent (see below)</i>	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 12:24
64	1	6508883.pn. <i>↳ or bent (see below)</i>	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 11:36
71	11	((6053980" or ("5879459" or ("5855681" or ("5820686" or ("5626677" or ("5442416" or ("4951601" or ("4801241" or ("4775281" or ("4566726" or ("4099041"))).PN.	USPAT;	2003/03/03 11:36
72	440	((glass or 'sio.sub.2' or "silicon dioxide" or silica or quartz) adj1 ((holder or rack or susceptor))) and (wafer or substrate or article) not (((wafer or substrate or article) with (shelves and (holder or rack or susceptor))) and robot)	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 12:11
86	3468	(118/728 or 118/729 or 118/108 or 156/345.31 or 156/345.32 or 156/345.51 or 156/345.52 or 156/345.53 or 156/345.54 or 156/345.55).ccls.	US-PGPUB; EPO; JPO; DERWENT; IBM TDB USPAT;	2003/03/03 12:12

219	19464	(boat or carrier or holder or rack or susceptor).ti. and (wafer or substrate or article).ti.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2003/03/03 15:23
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247	1243	((glass or 'sio.sub.2' or "silicon dioxide" or silica or quartz) with jig) and (wafer or substrate or article)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM 'TDB	2003/03/03 15:46
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